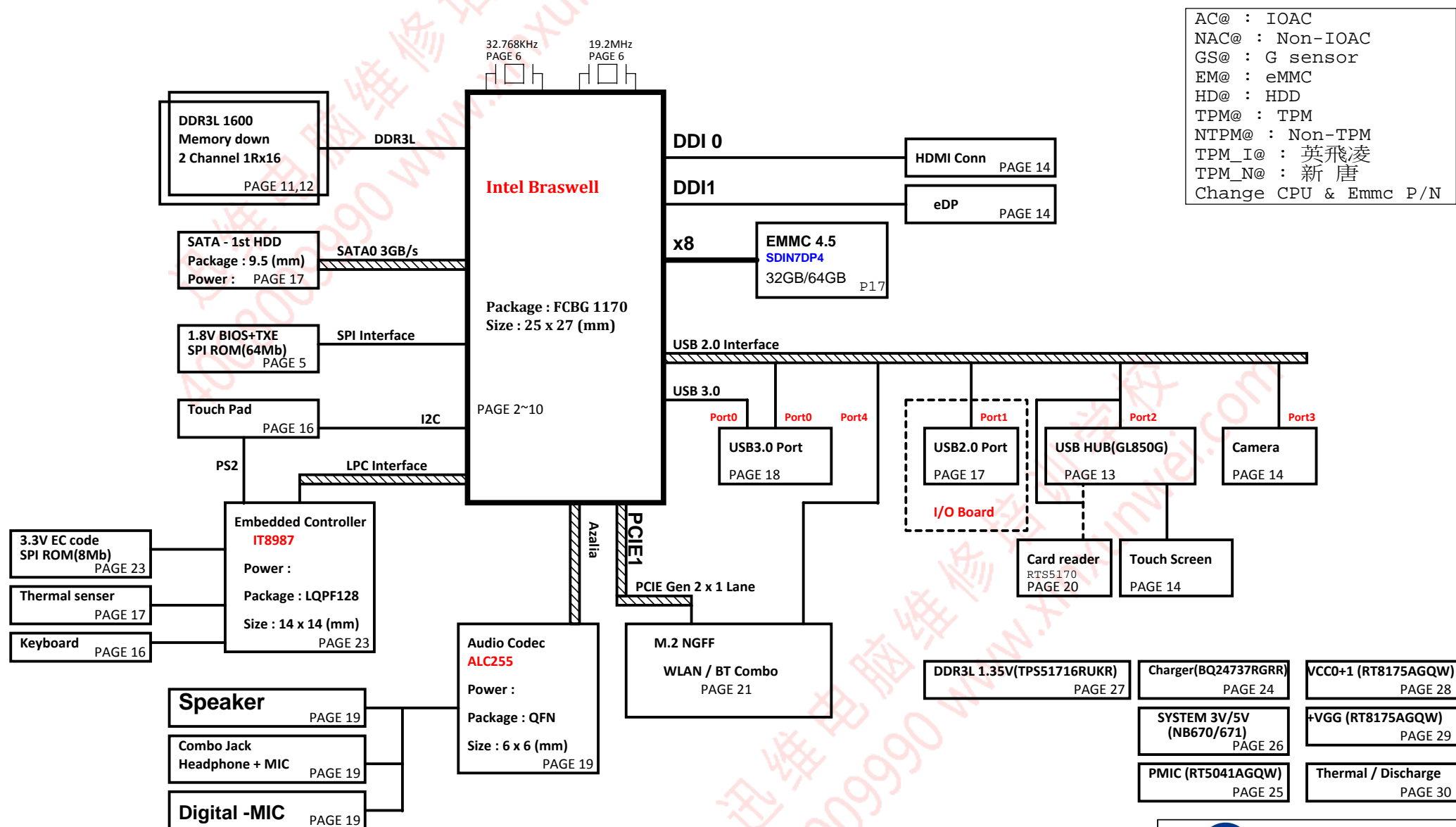
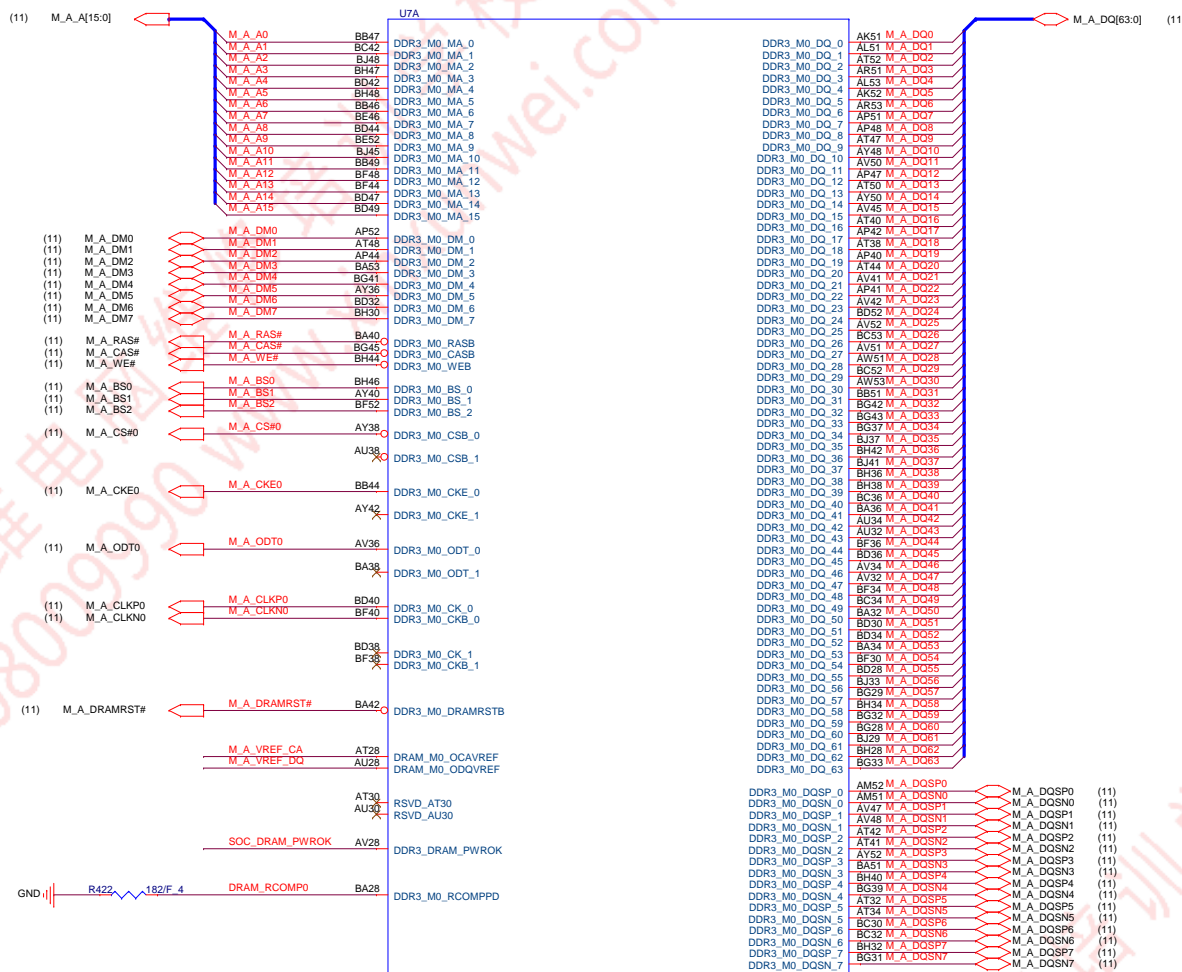


ZHX_ZHXS UMA(11.6")

Intel Braswell Platform Block Diagram

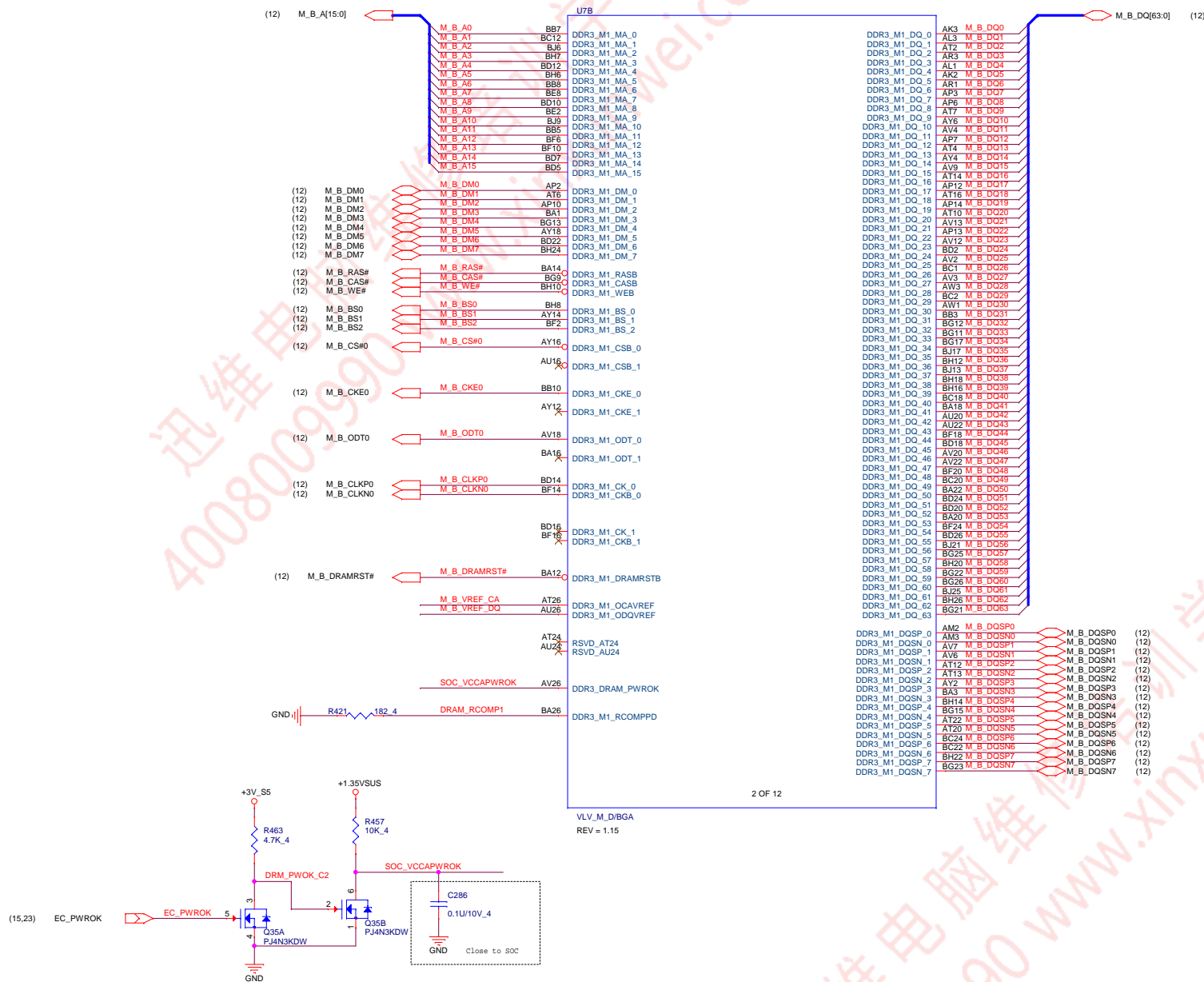


+1.35VSUS (3,9,11,12,22,27)
+3V_S5 (3,5,9,13,15,16,18,23,25)



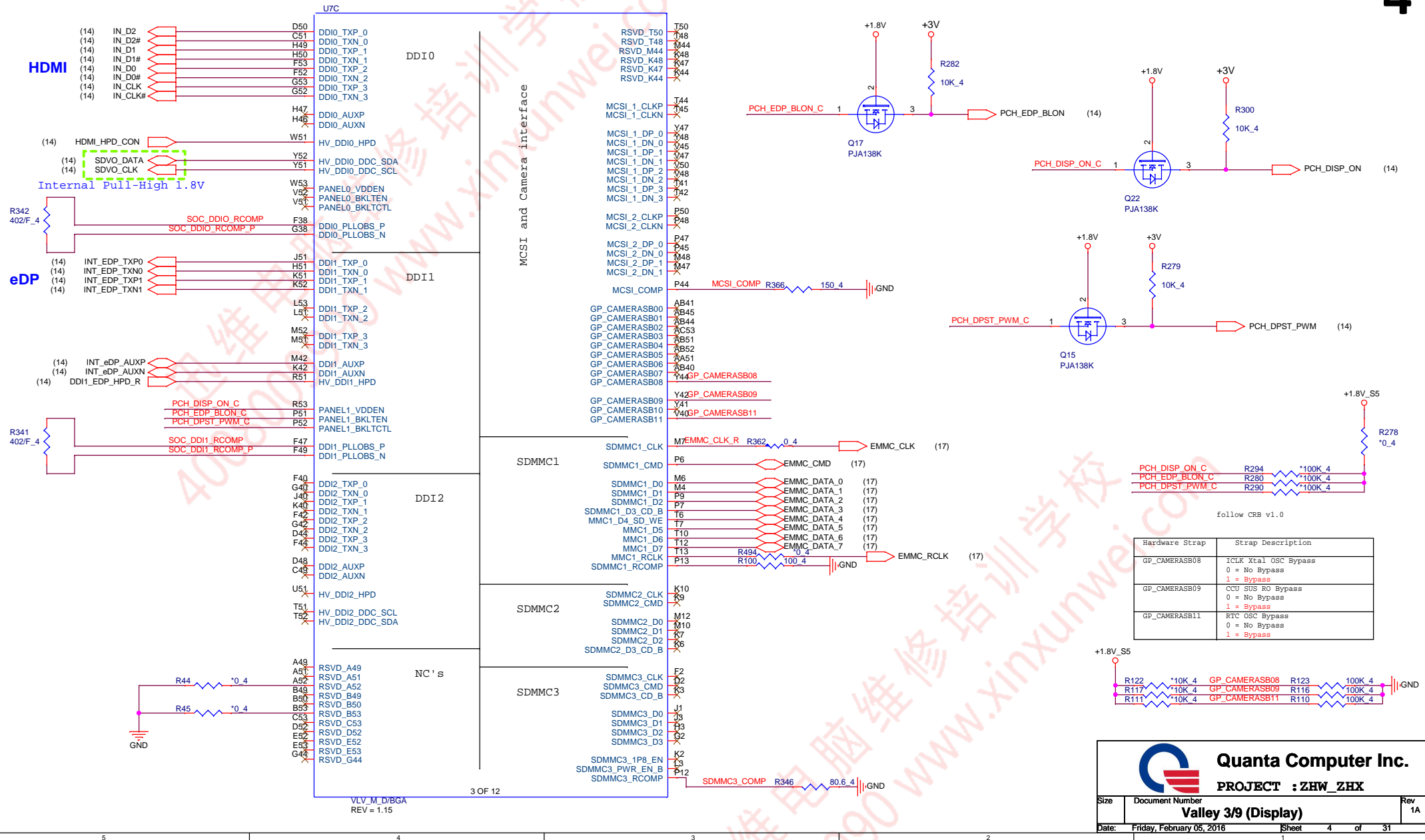
Channel 0	Channel 1	SOC Supported Memory Operation Speed
1333 MHz	X	1066 MHz
1600 MHz	X	1600 MHz
1333 MHz	1333 MHz	1066 MHz
1600 MHz	1600 MHz	1600 MHz

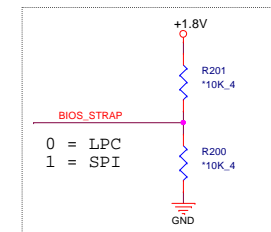
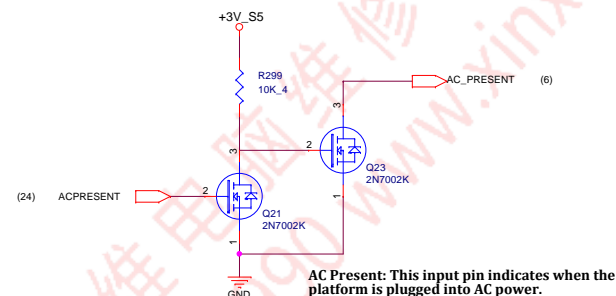
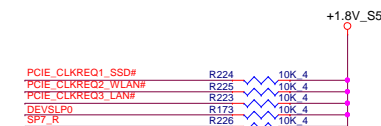
Channel 0 need to be populated first for the platform to power on

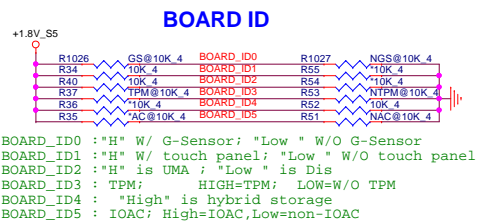
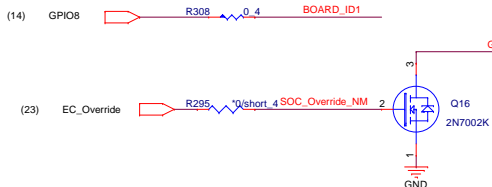
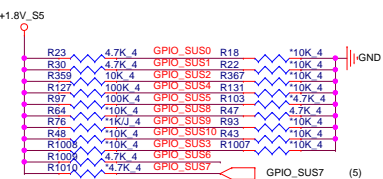


(7,9,13,14,15,16,17,18,19,20,21,22,23,26,27,28,29,30)

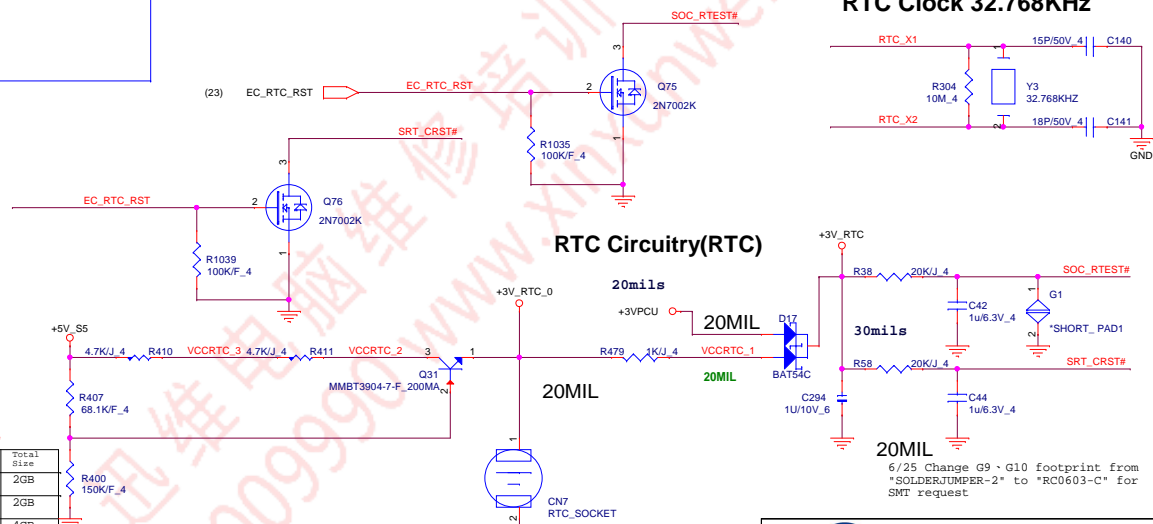
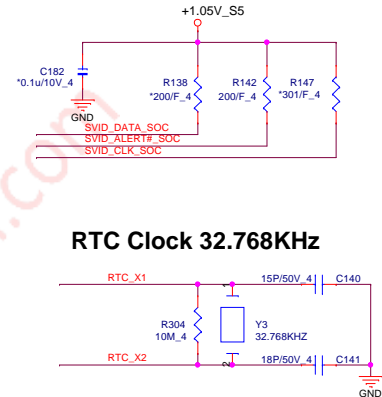
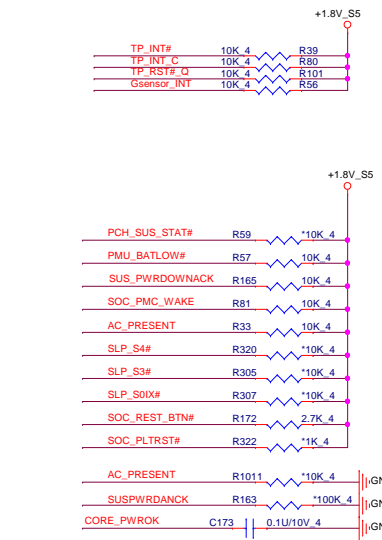
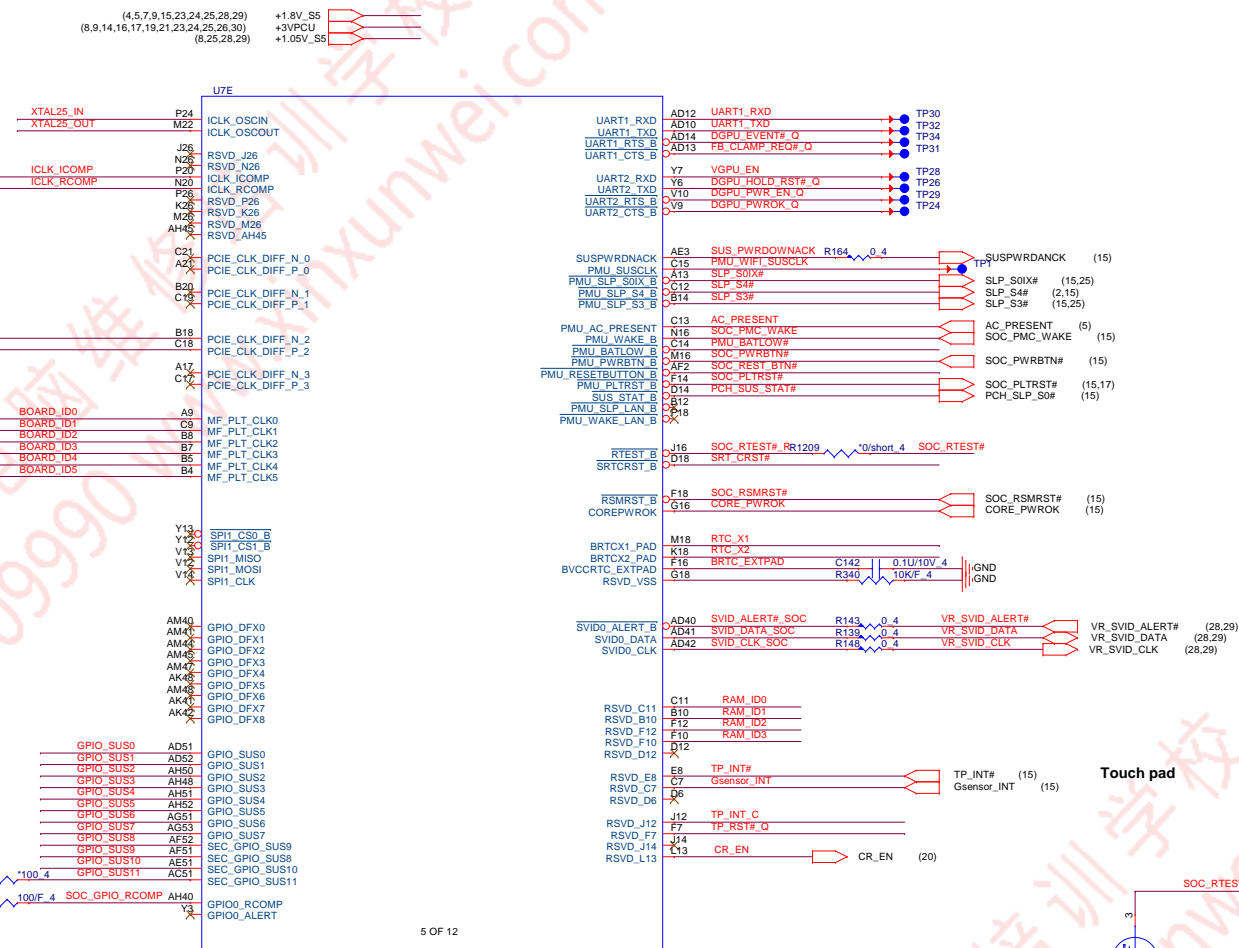
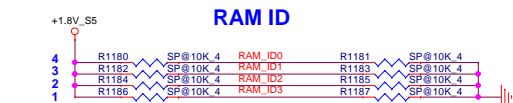
+3V

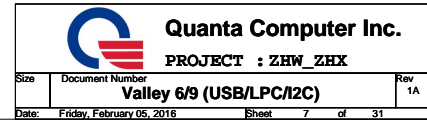


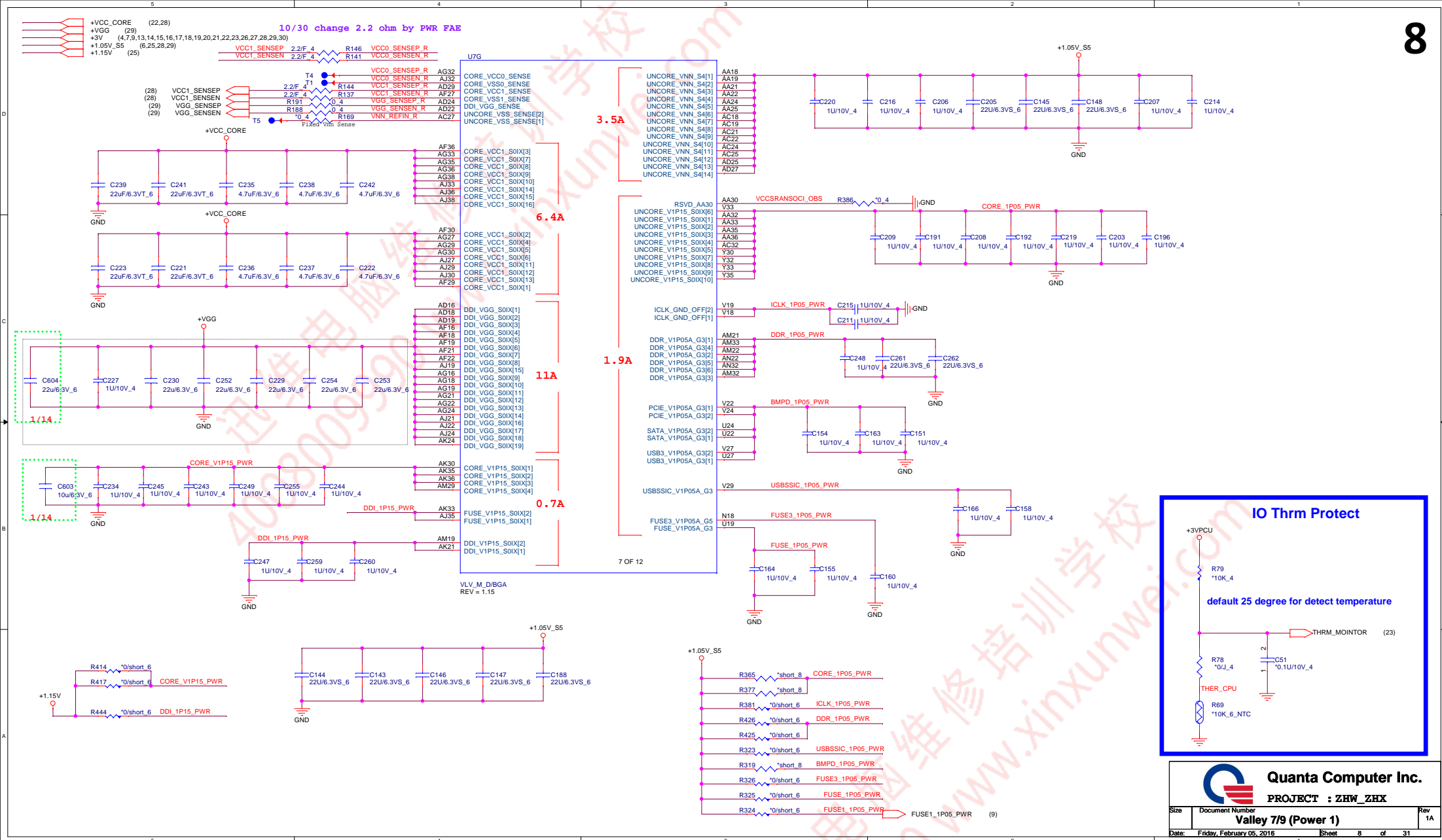


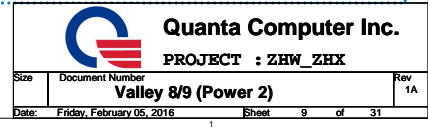


Vendor	RAM_ID	Q PN	Mfr. PN	Freq.	Size	Total Size
Hynix	0000	AKD5PGSTW13	H5TC4G63CFR-PBA	1600MHz	4Gb	2GB
Samsung	0001	AKD5JG0T504	K4B4G1646E-BYK0	1600MHz	4Gb	2GB
Hynix	0010	AKD5PGSTW13	H5TC4G63CFR-PBA	1600MHz	4Gb	4GB
Samsung	0011	AKD5JG0T504	K4B4G1646E-BYK0	1600MHz	4Gb	4GB
	1234					











DDR3L MEMORY CHANNEL A

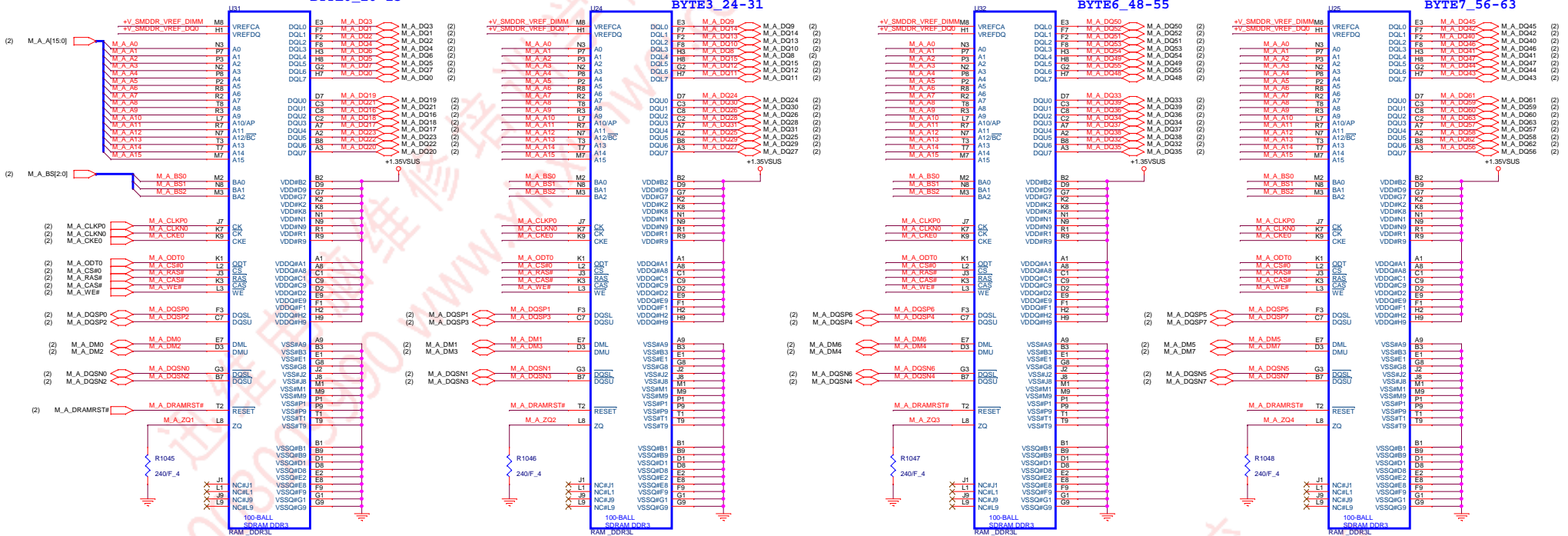
BYTE0_0-7
BYTE0_16-23

BYTE0_8-15
BYTE3_24-31

BYTE4_32-39
BYTE6_48-55

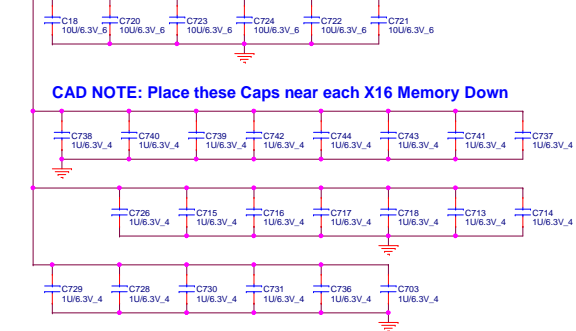
BYTE5_40-47
BYTE7_56-63

11

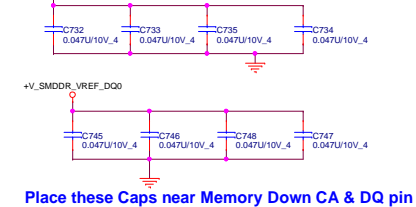


DE-CAPS FOR MEMORY CHANNEL A

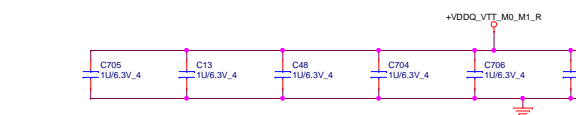
CAD note: Distributed around all DRAM devices (CHA)



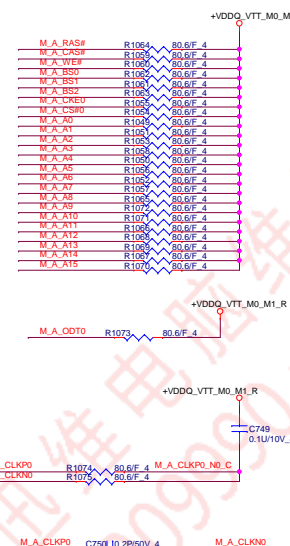
PLACE 2 CAPS NEAR EACH DDR3L IC



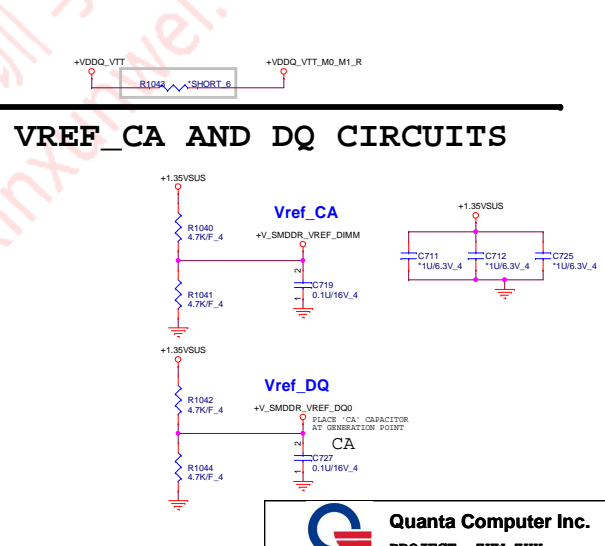
Place these Caps near Memory Down CA & DQ pin



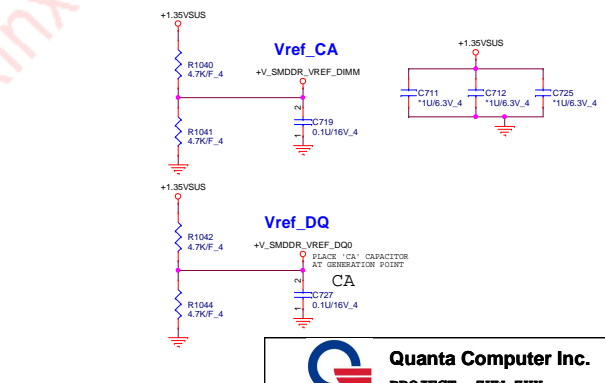
VTT TERMINATIONS



VOLTAGE MERGE



VREF_CA AND DQ CIRCUITS

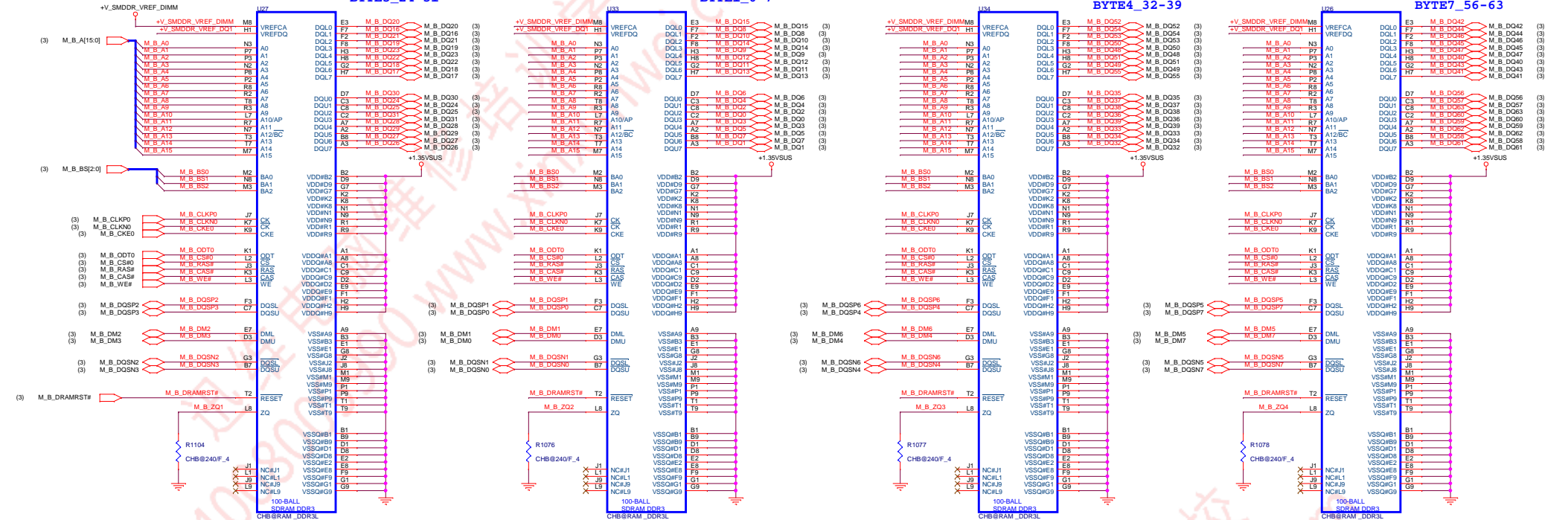


BYTE2_16-23
BYTE3_24-31

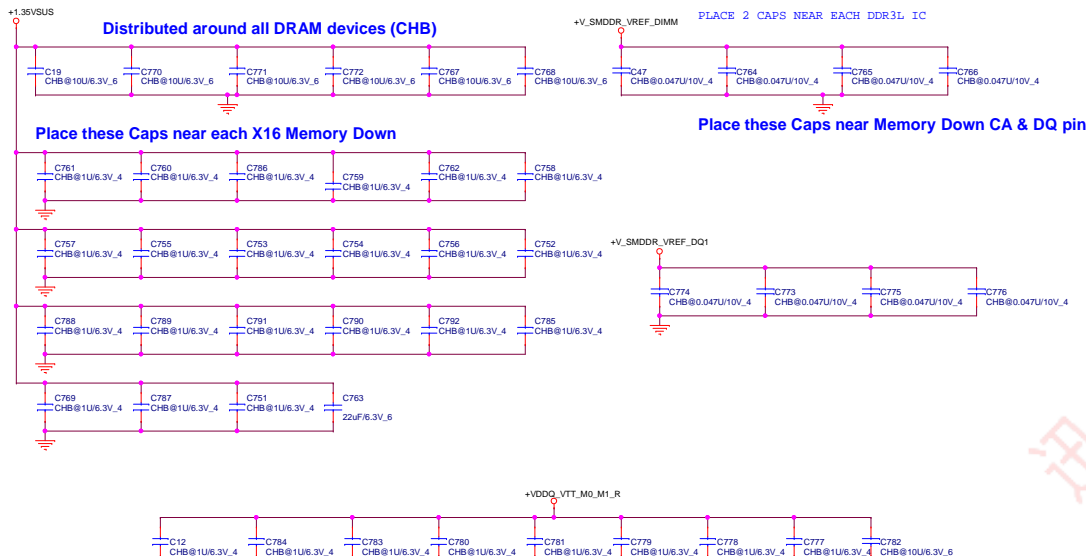
BYTE0_8-15
BYTE1_0-7

BYTE6_48-55
BYTE4_32-39

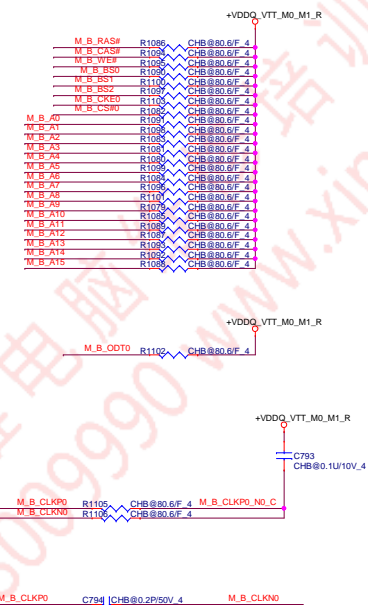
BYTE5_40-47
BYTE7_56-63



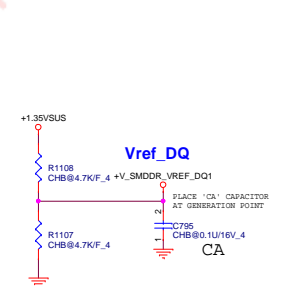
DE-CAPS FOR MEMORY CHANNEL B

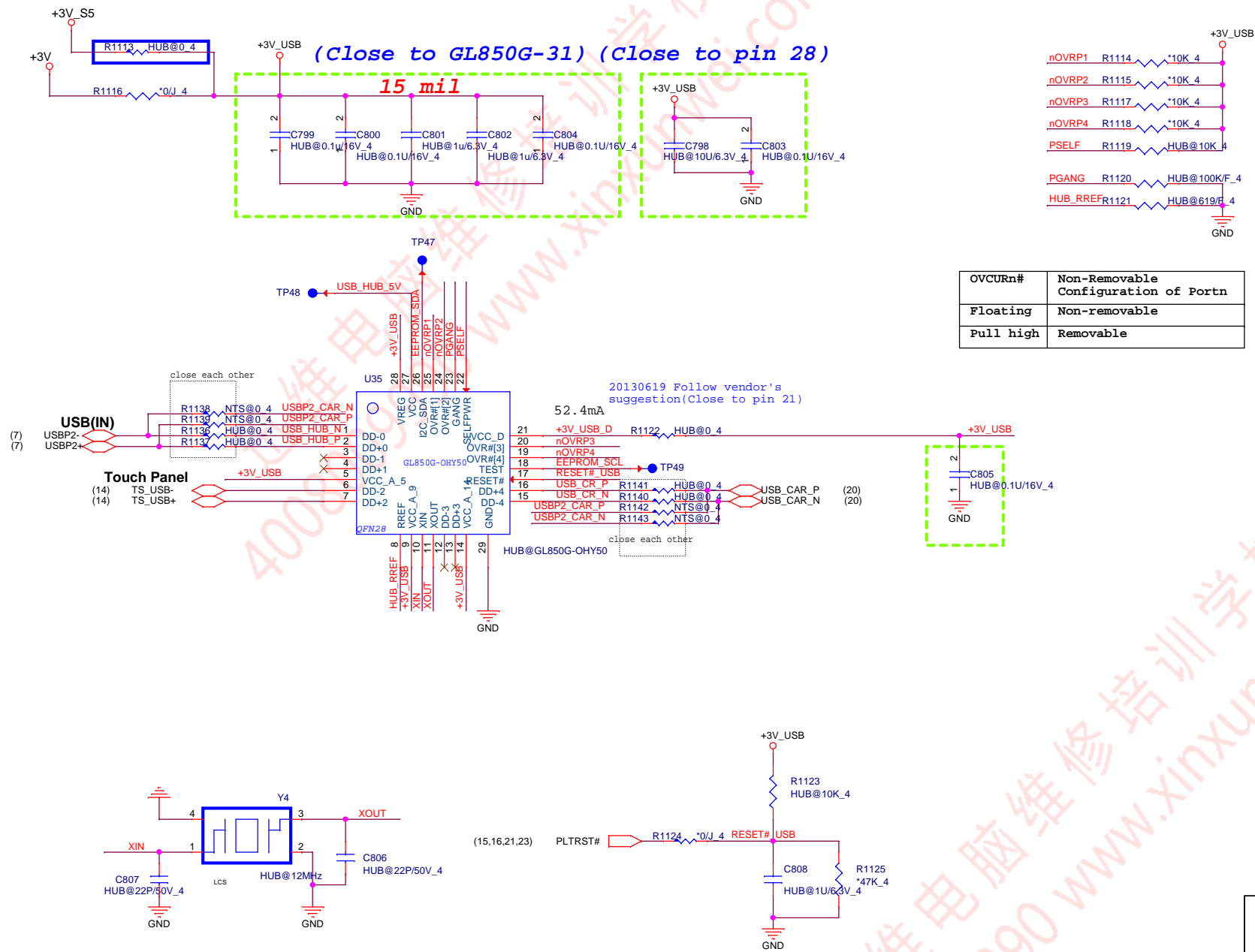


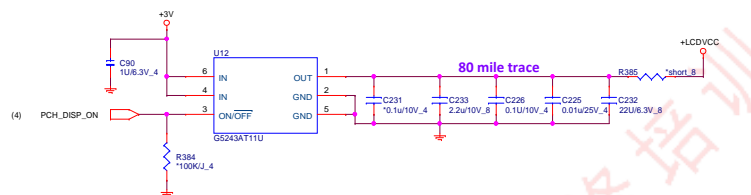
VTT TERMINATIONS



VREF_DQ CIRCUIT

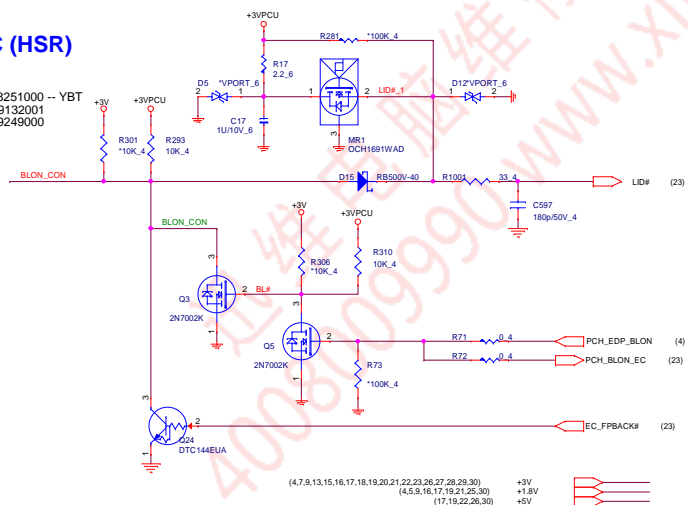




LVDS Conn.

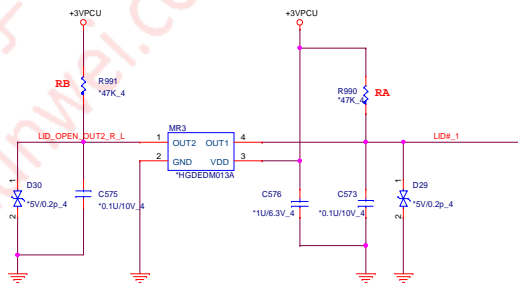
HALL IC (HSR)

1st source : EOD
2nd source : AL008251000 -- YBT
3rd source : AL009132001
4th source : AL009249000

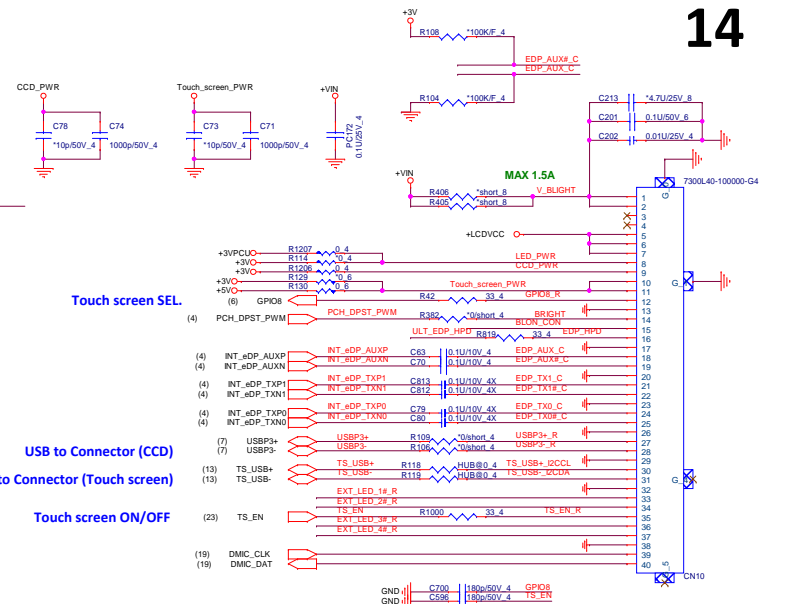


GMR Sensor

RA/RB can be unstuffed if using GMR



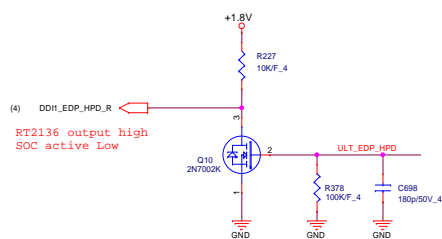
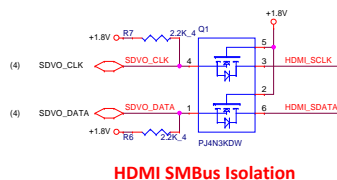
Touch screen SEL.



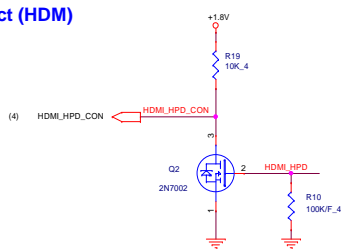
USB to Connector (CCD)

USB to Connector (Touch screen)

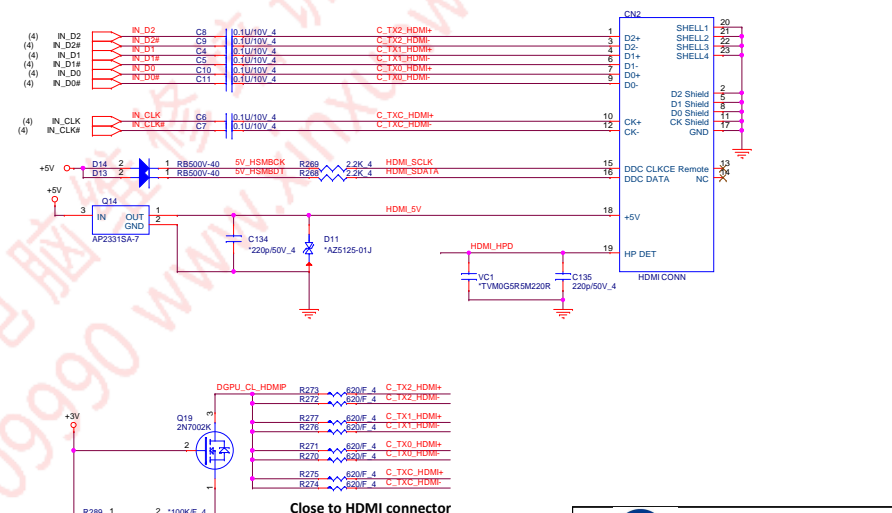
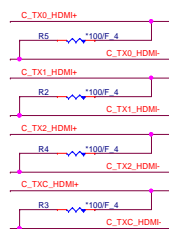
Touch screen ON/OFF

**HDMI Conn.**

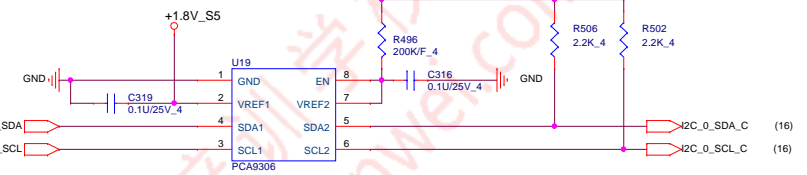
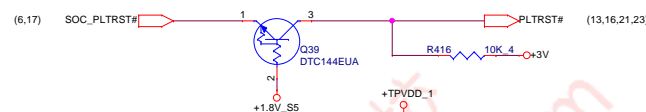
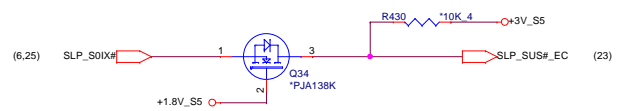
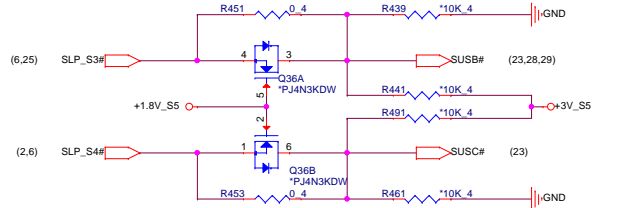
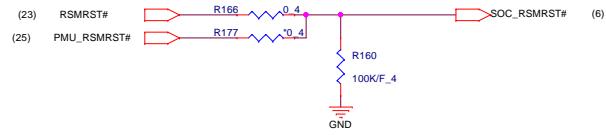
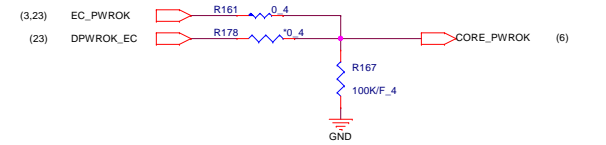
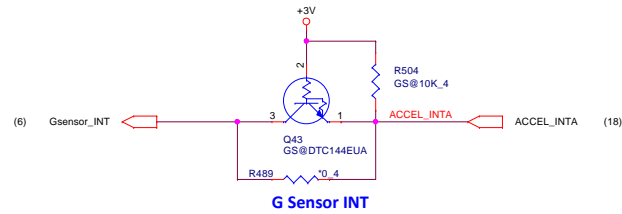
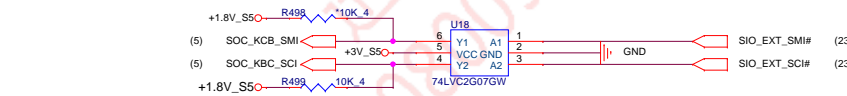
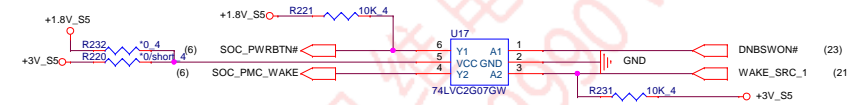
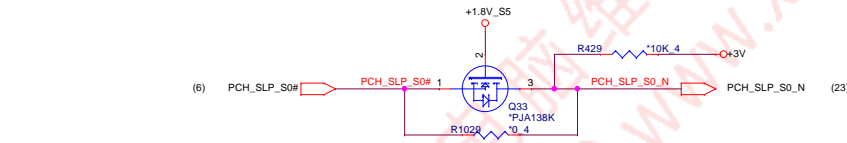
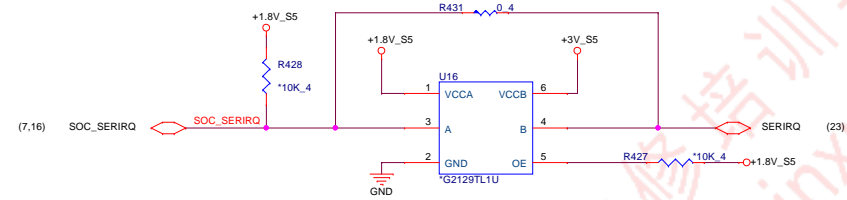
HDMI-detect (HDM)



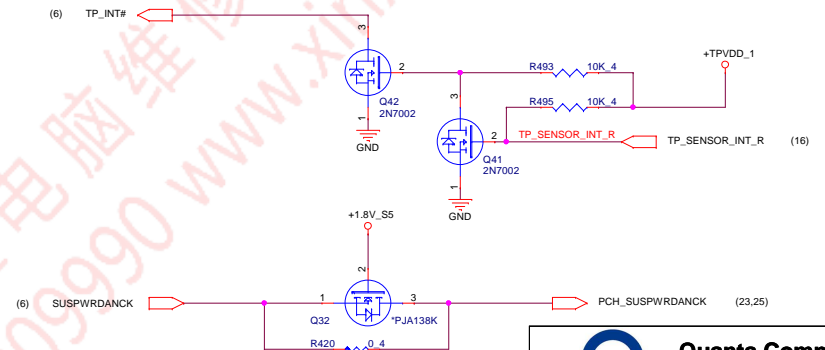
EMI (EMC)



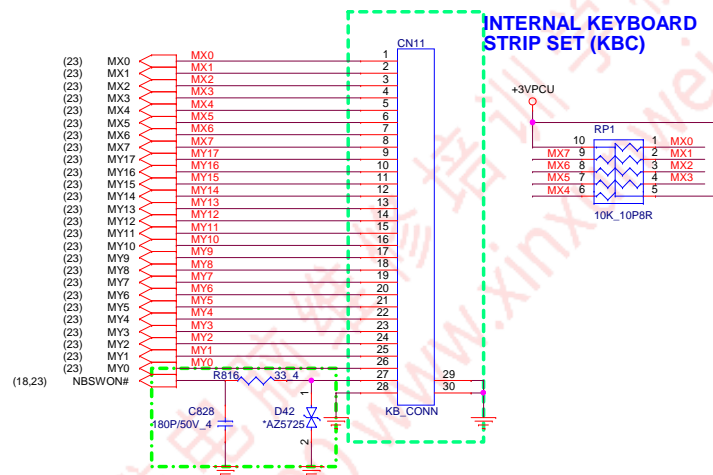
+1.8V_S5 (4,5,6,7,9,23,24,25,28,29)
 +3V_S5 (2,3,5,9,13,16,18,23,25)
 +1.8V (4,5,9,14,16,17,19,21,25,30)
 +3V (4,7,9,13,14,16,17,18,19,20,21,22,23,26,27,28,29,30)



For Touch pad : POWER-A

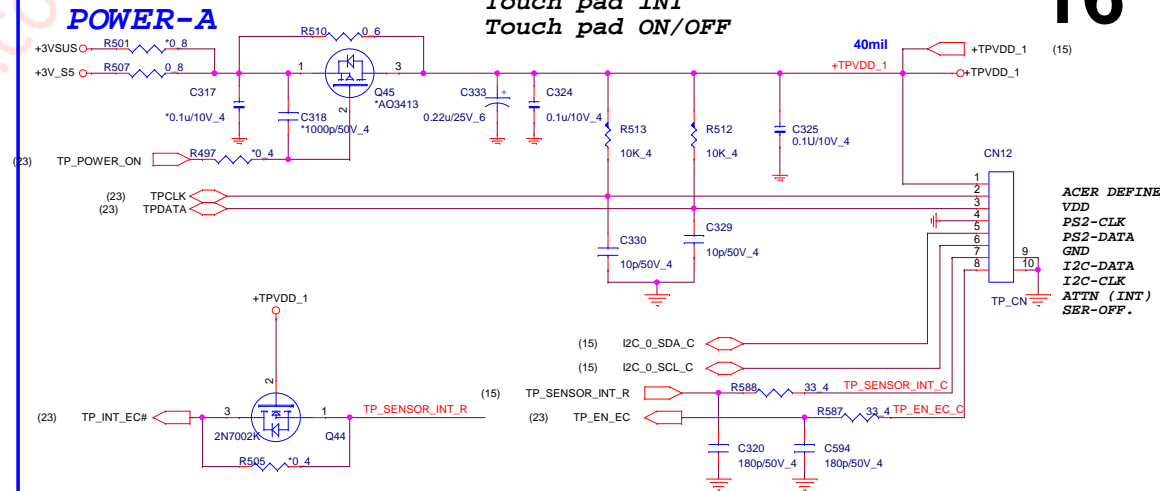


KEYBOARD (KBC)

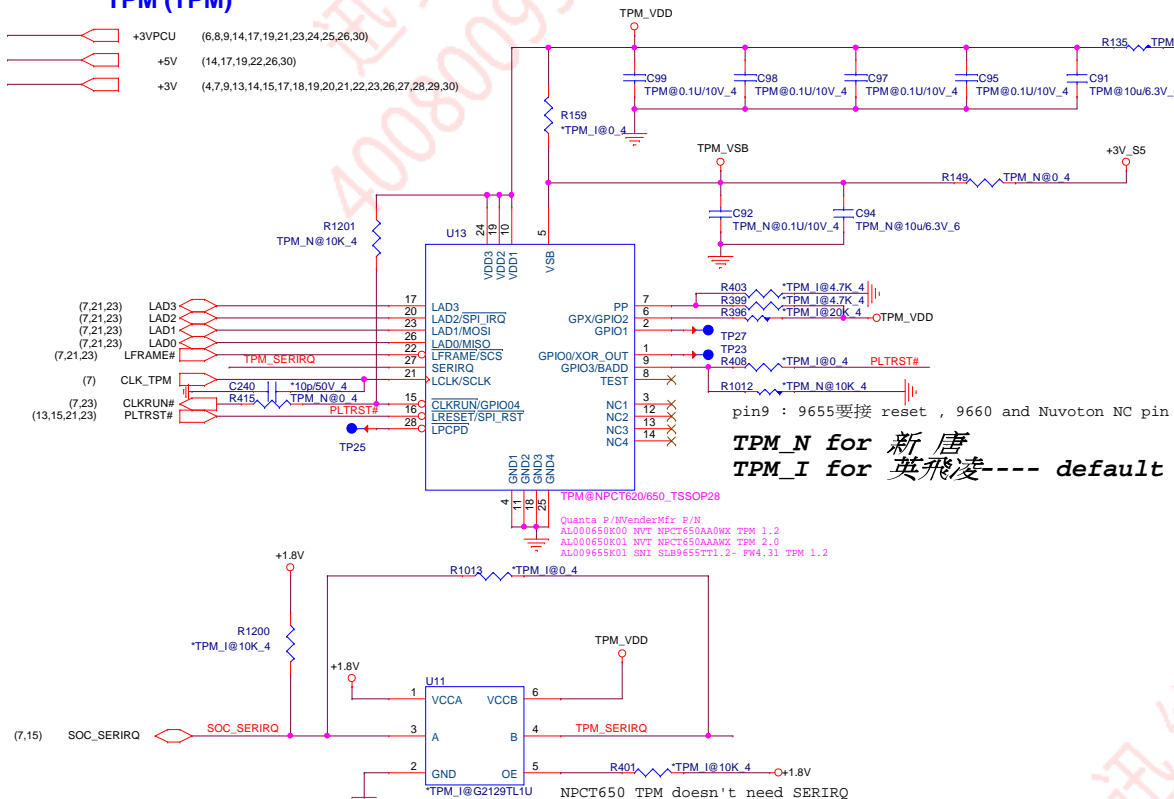


TOUCH PAD (TPD)

Touch pad I2C
Touch pad INT
Touch pad ON/OFF

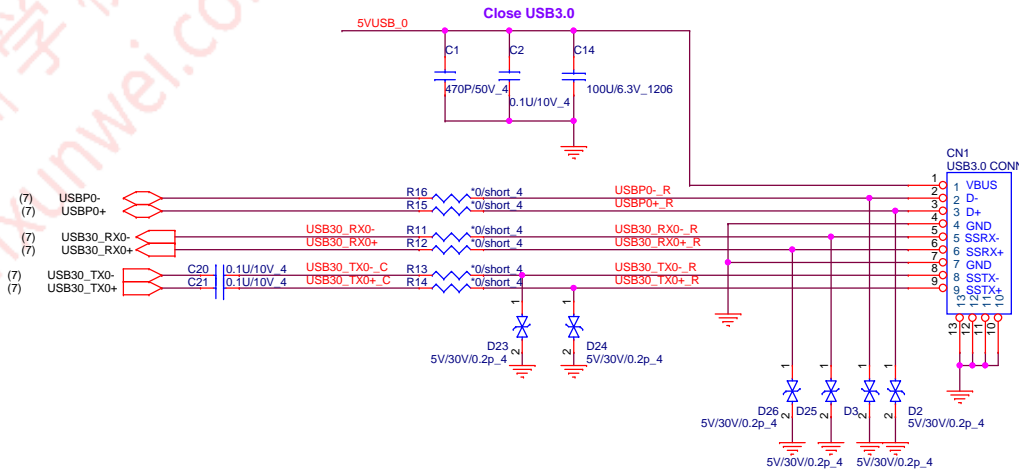
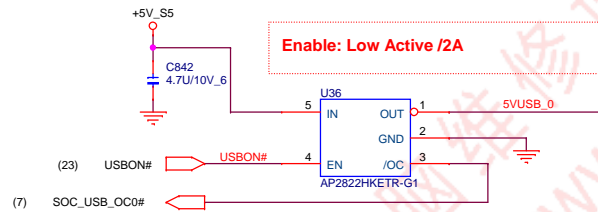


TPM (TPM)

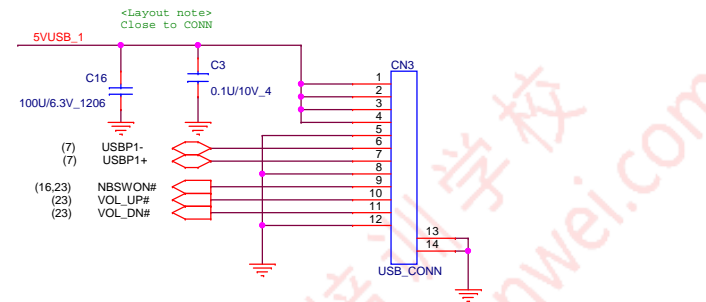
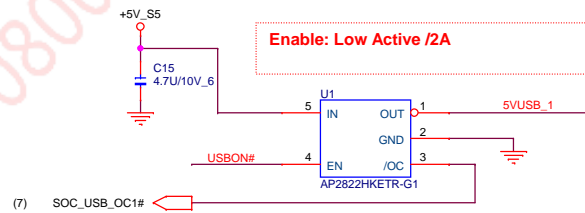


note: serie need to add level shift

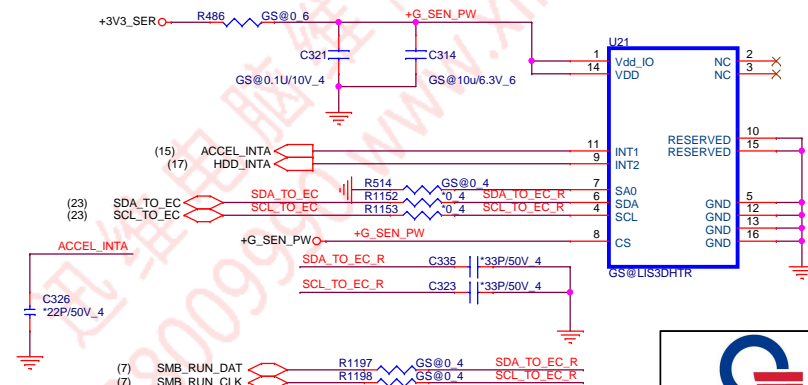
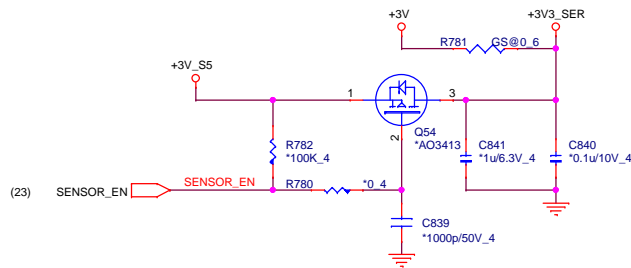
USB 3.0 Connector



D/B Port USB 2.0



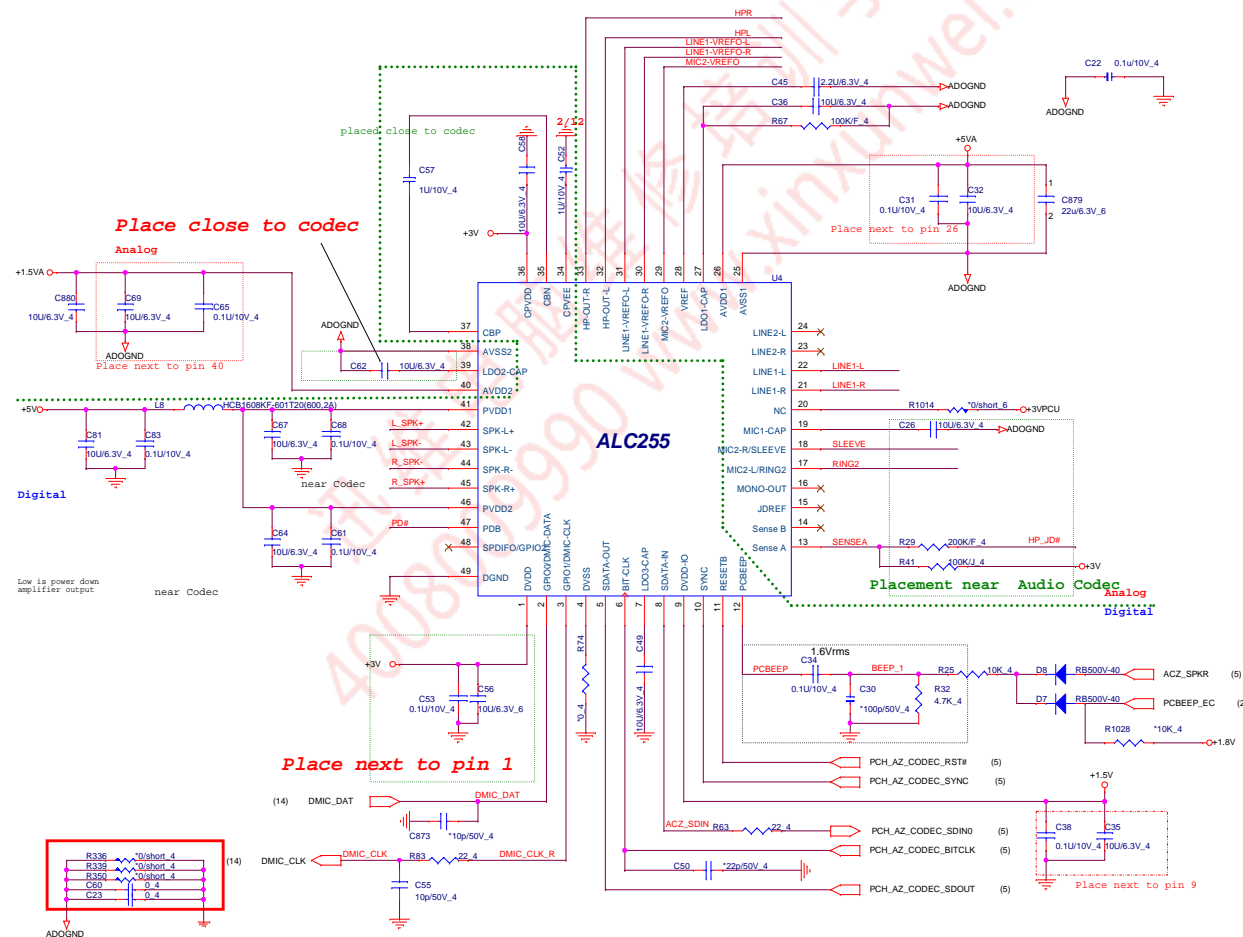
G-sensor



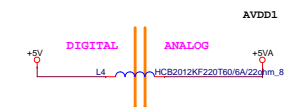
Codec(ADO)

(14,17,22,26,30)

+5V



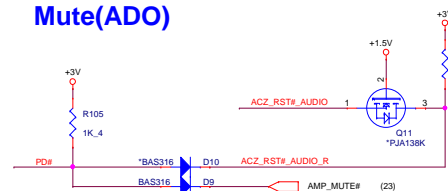
Codec PWR 5V(ADO)



Codec PWR 1.5V(ADO)



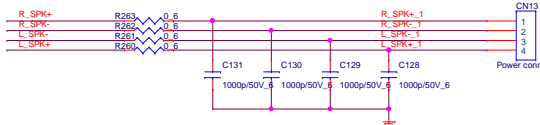
Mute(ADO)



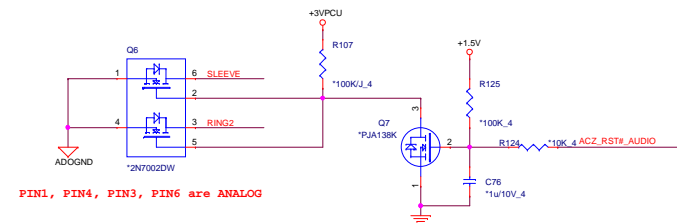
Internal Speaker

footprint 88266-040xx-xxx-4p-1

40mil for each signal



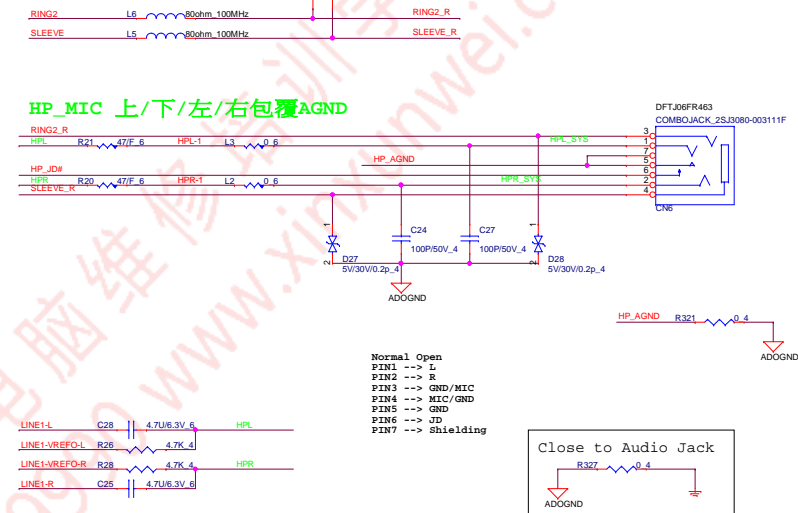
Grounding circuit(ADO)

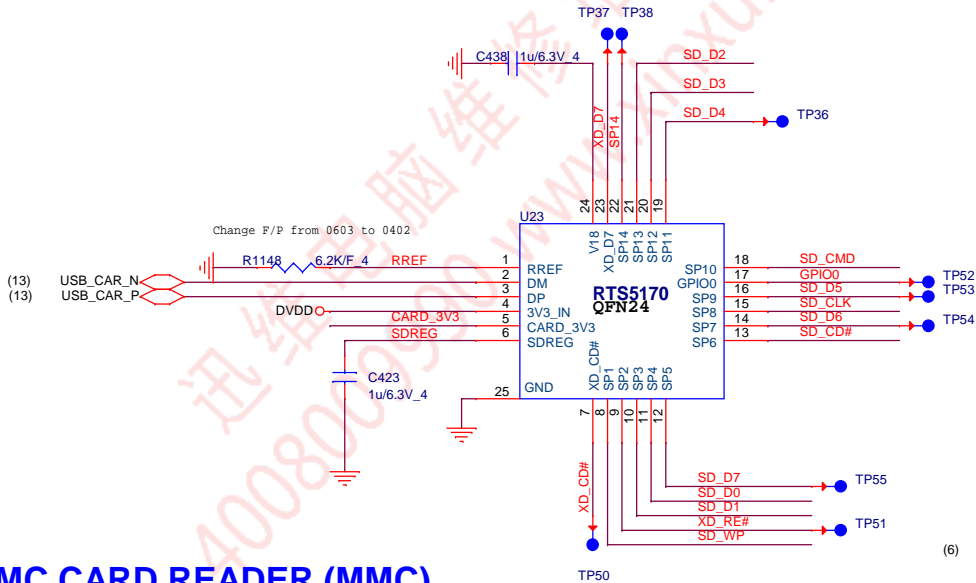


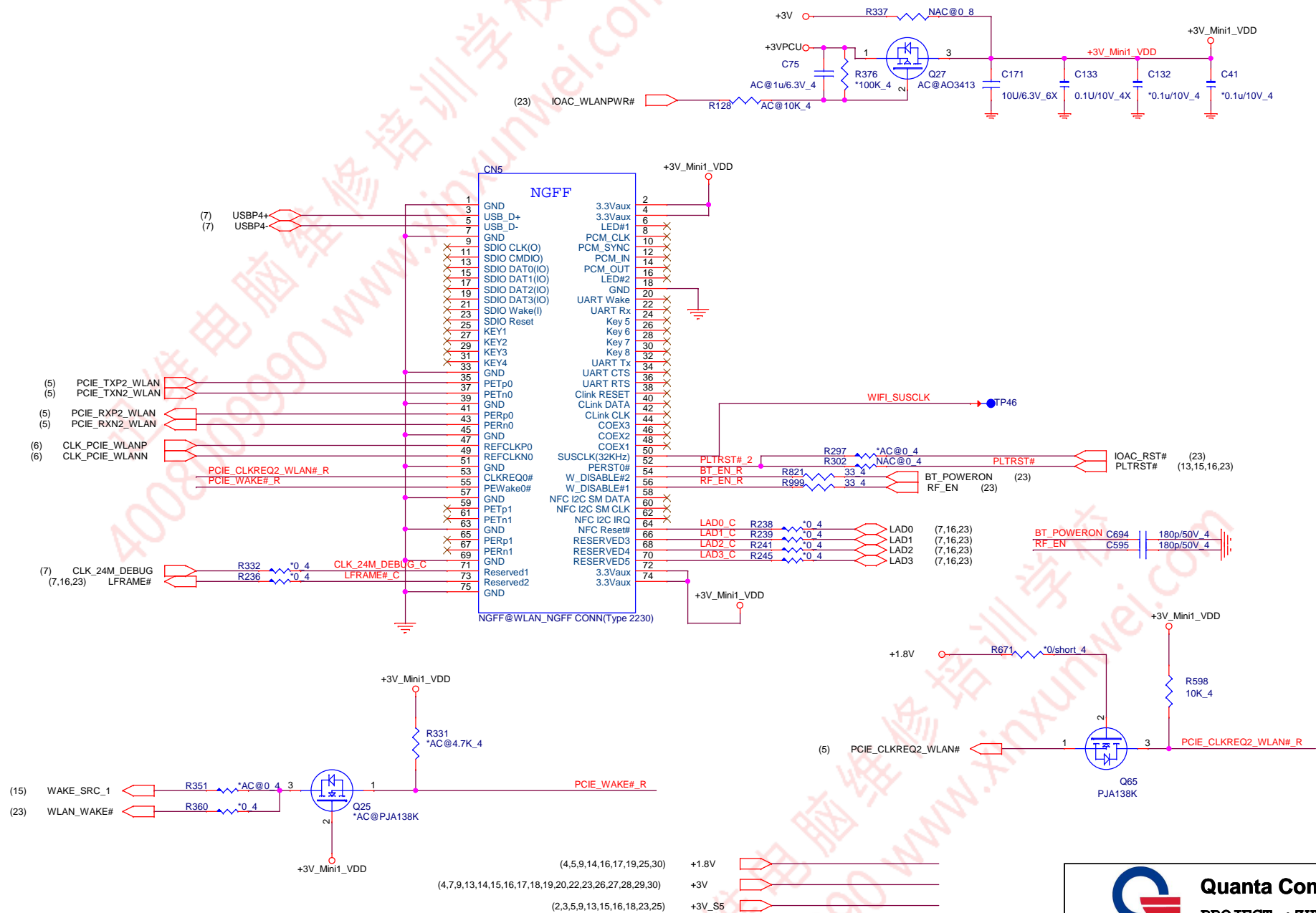
Microphone

move to LED BD

note : change next P/N: DFTJ06FR653
CONN DIP PHONE JACK 6P FR(H4.5)
foot print: phjk-2sj3072-108111f-6p



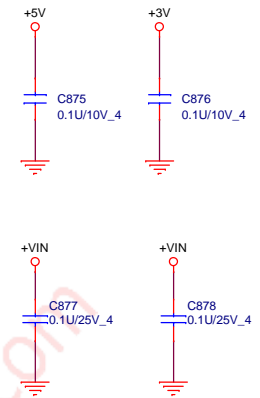
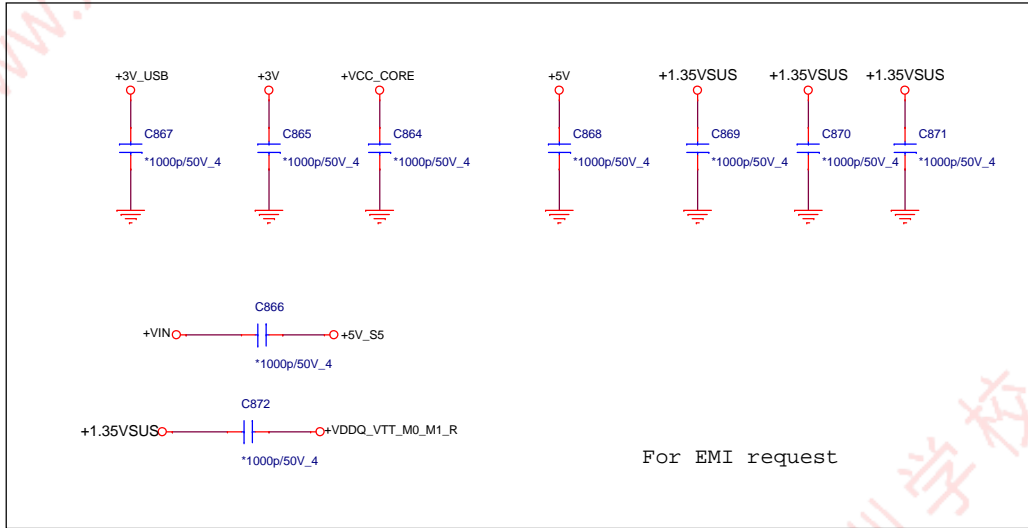
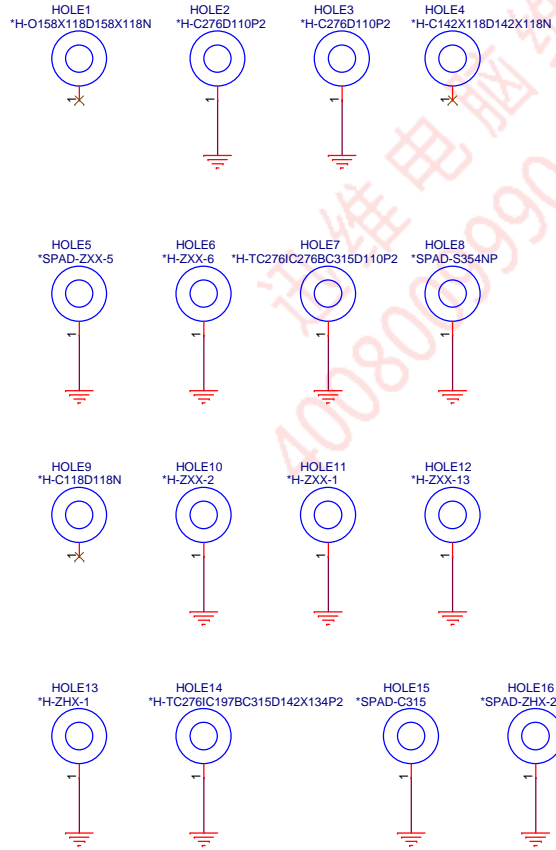




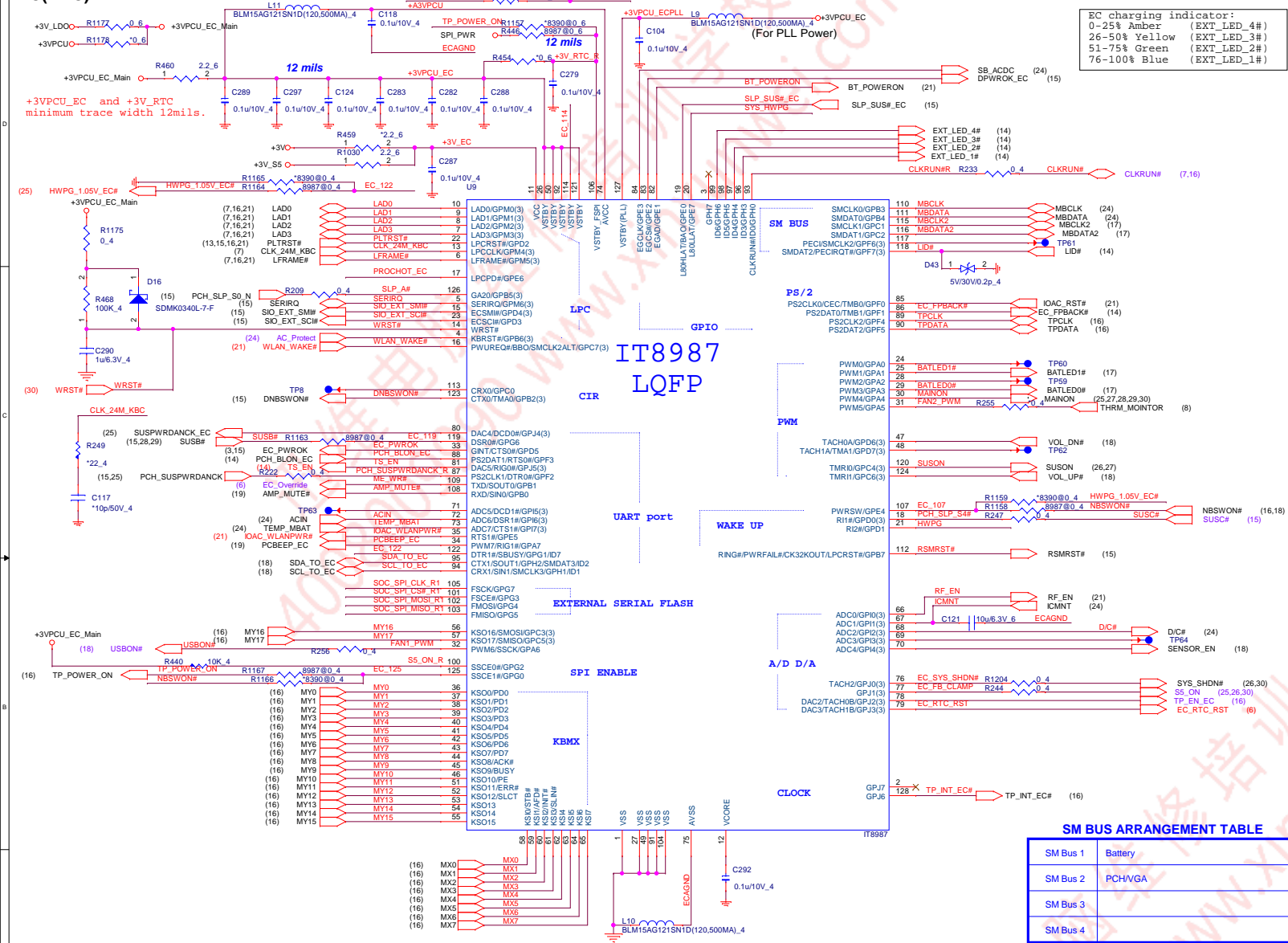
Quanta Computer Inc.

PROJECT : ZHW_ZHX

Size	Document Number	Rev
	WIFI & BT	1A
Date:	Friday, February 05, 2016	Sheet 21 of 31

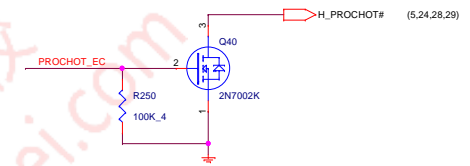
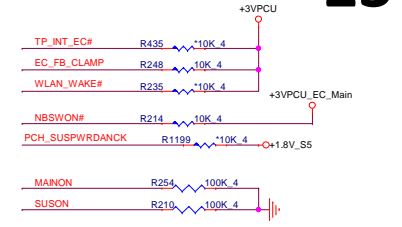


EC(KBC)

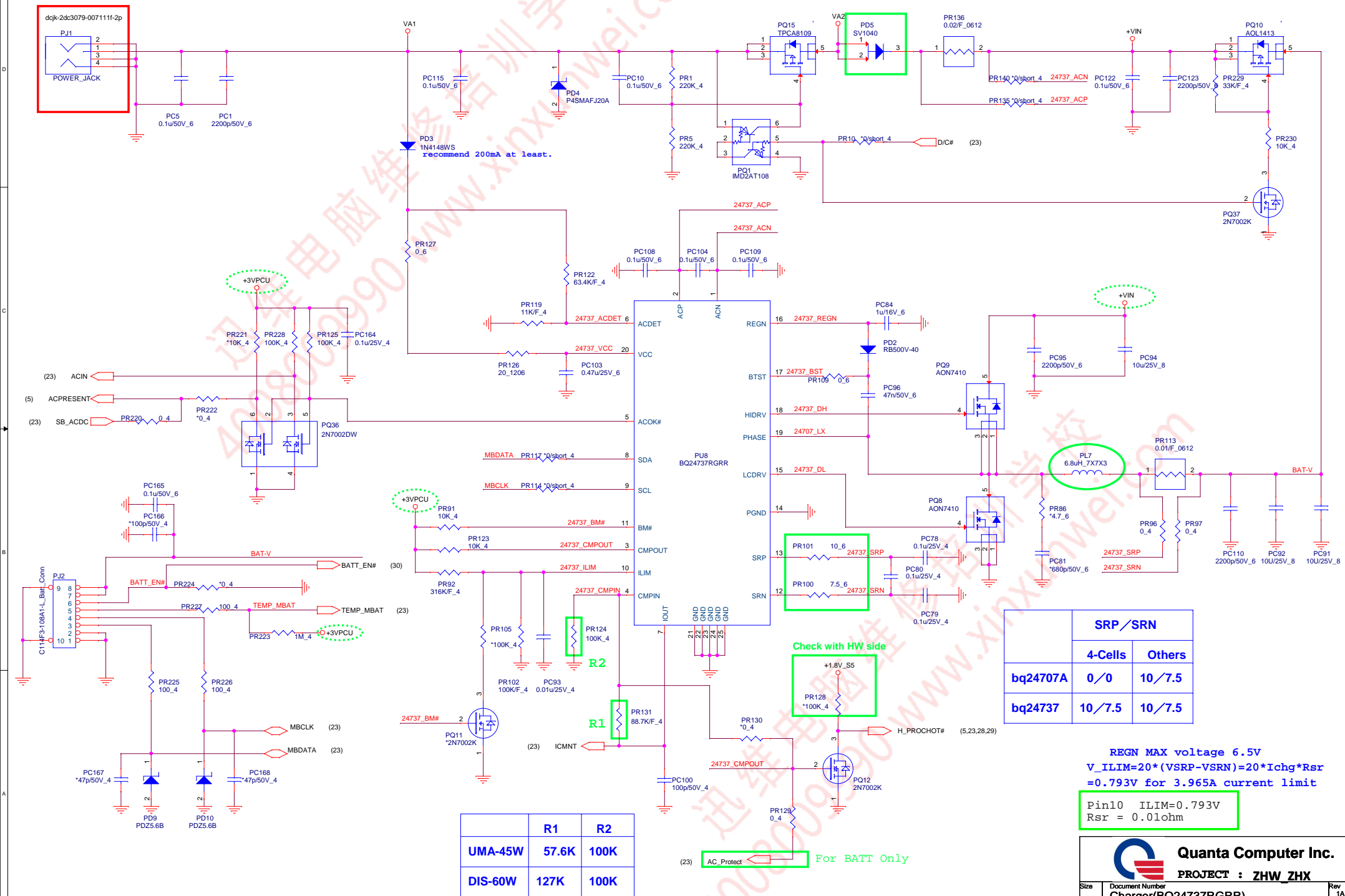


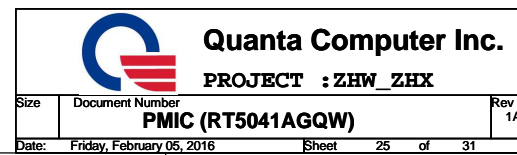
SM BUS PU(KBC)

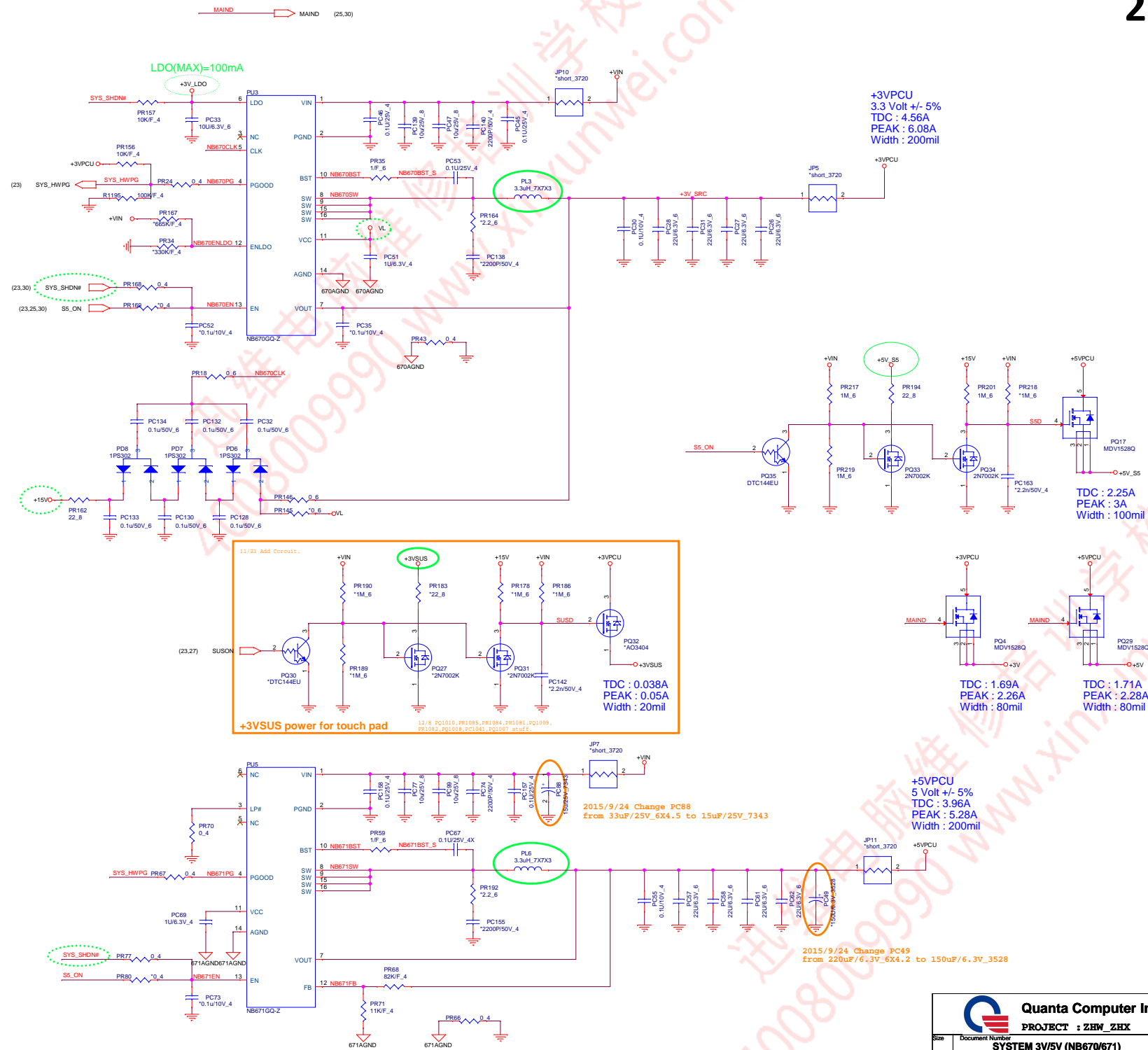
HWPG(KBC)



Check DC Jack Type



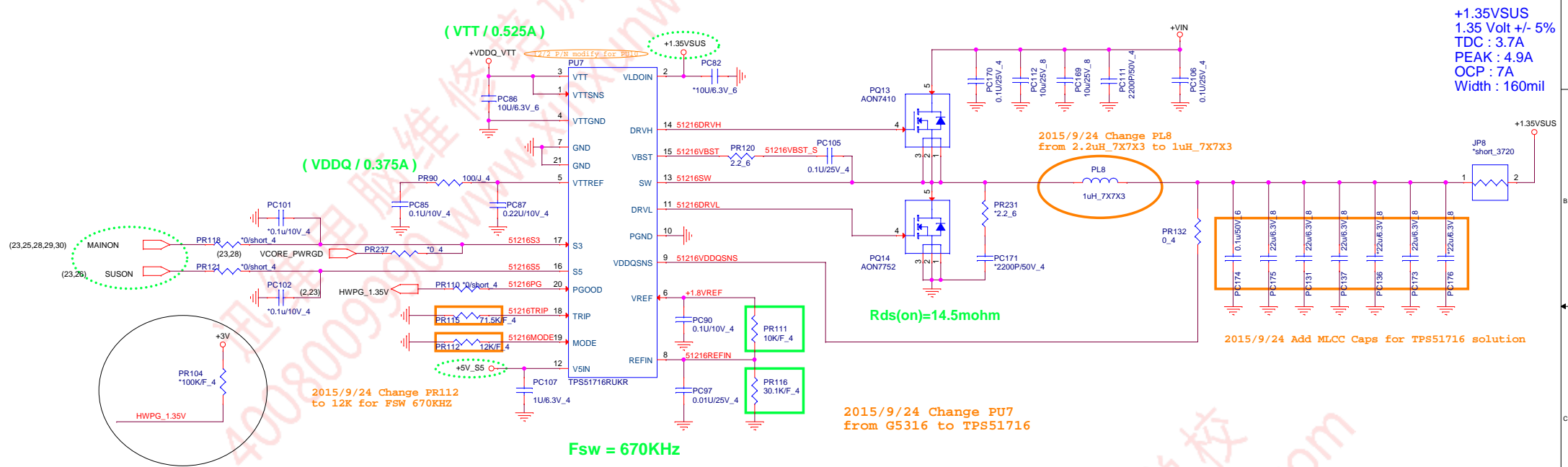




(2,3,9,11,12,22)
(11)
(6,18,22,26,28,29)

+1.35VSUS
+VDDQ_VTT
+5V_S5

The diagram shows three power supply pins connected to a device. The pins are labeled +1.35VSUS, +VDDQ_VTT, and +5V_S5. The device pins are labeled (2,3,9,11,12,22), (11), and (6,18,22,26,28,29). The connections are shown as three horizontal lines with arrows pointing to the right, indicating the power supply pins.



```
OCP=7A
L ripple current
=(19-1.35)*1.35/(1u*670k*19)
=1.871A
Vtrip=7-(1.871/2)*14.5mohm
=87.935mV
Rlimit=87.935mV/10uA*8=70.34Kohm
```

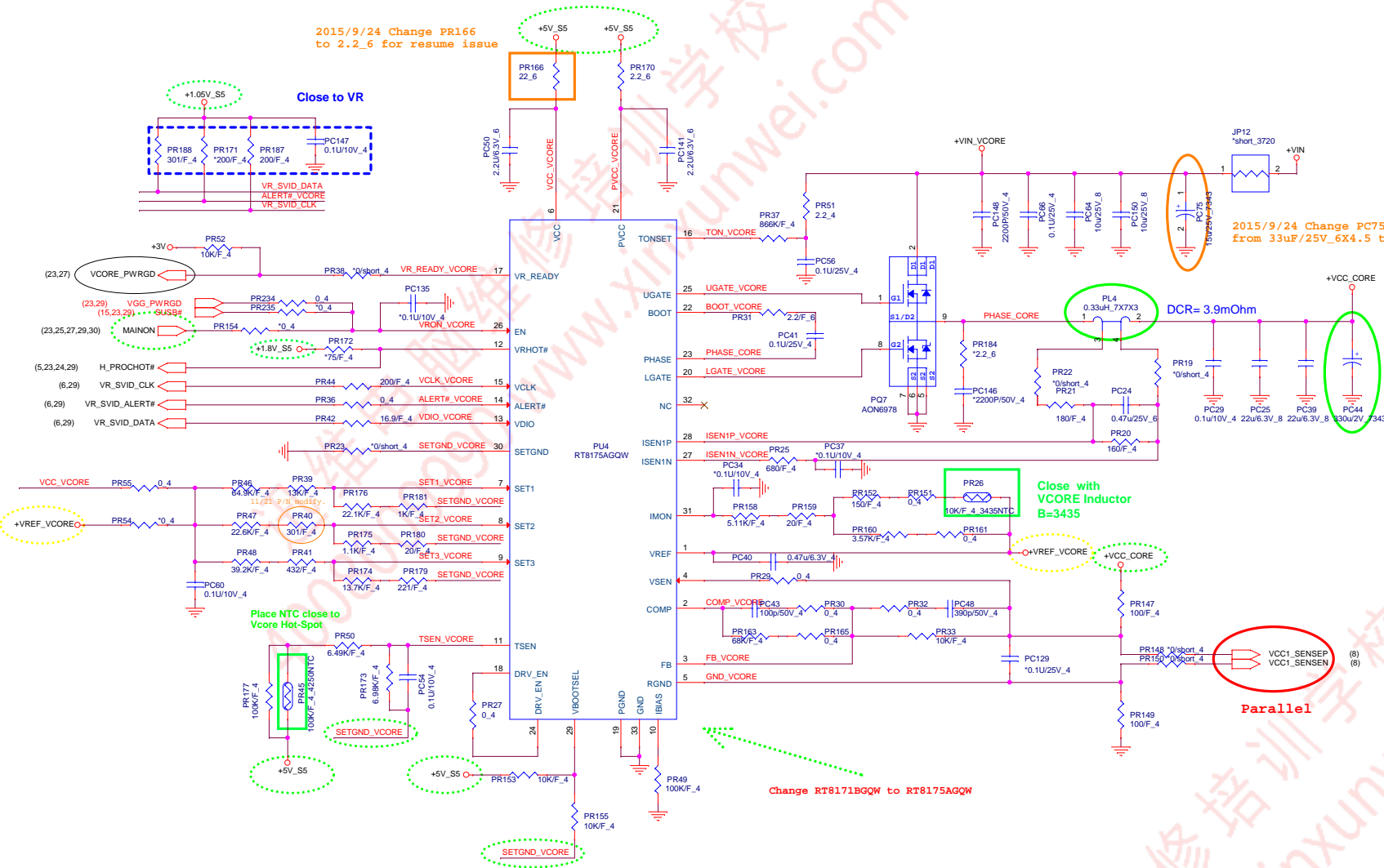
```
DDR=1.35V
PR111=10K/F_4
PR116=30.1K/F_4
```

Mode	Frequency	Discharge mode
12K	670K	Tracking Discharge
1K	500K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

2015/9/24 Change PR166
to 2.2.6 for resume issue

Close to VR



2015/9/24 Change PR108
to 2.2_6 for resume issue

Close to VR

VR_READY_VGG

VR 12.1

Braswell - VGG (1 Phase)

Icc TDC PL2 : TBD

Icc Max : 15A

OCP : 20.7A

Fsw : 800KHz

VR Address : 5

VCORE L/L :

R_DC_LL : 0 mV/A


R_AC_LL : 0 mV/A

Place NTC close to
Vcore Hot-Spot

Close with
VCORE Inductor
B=3435

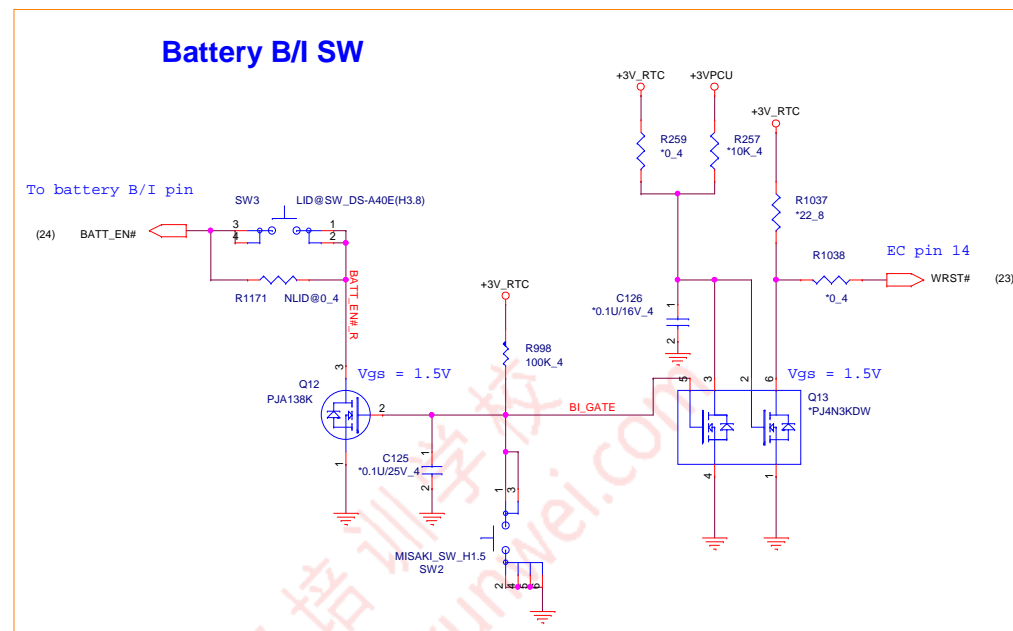
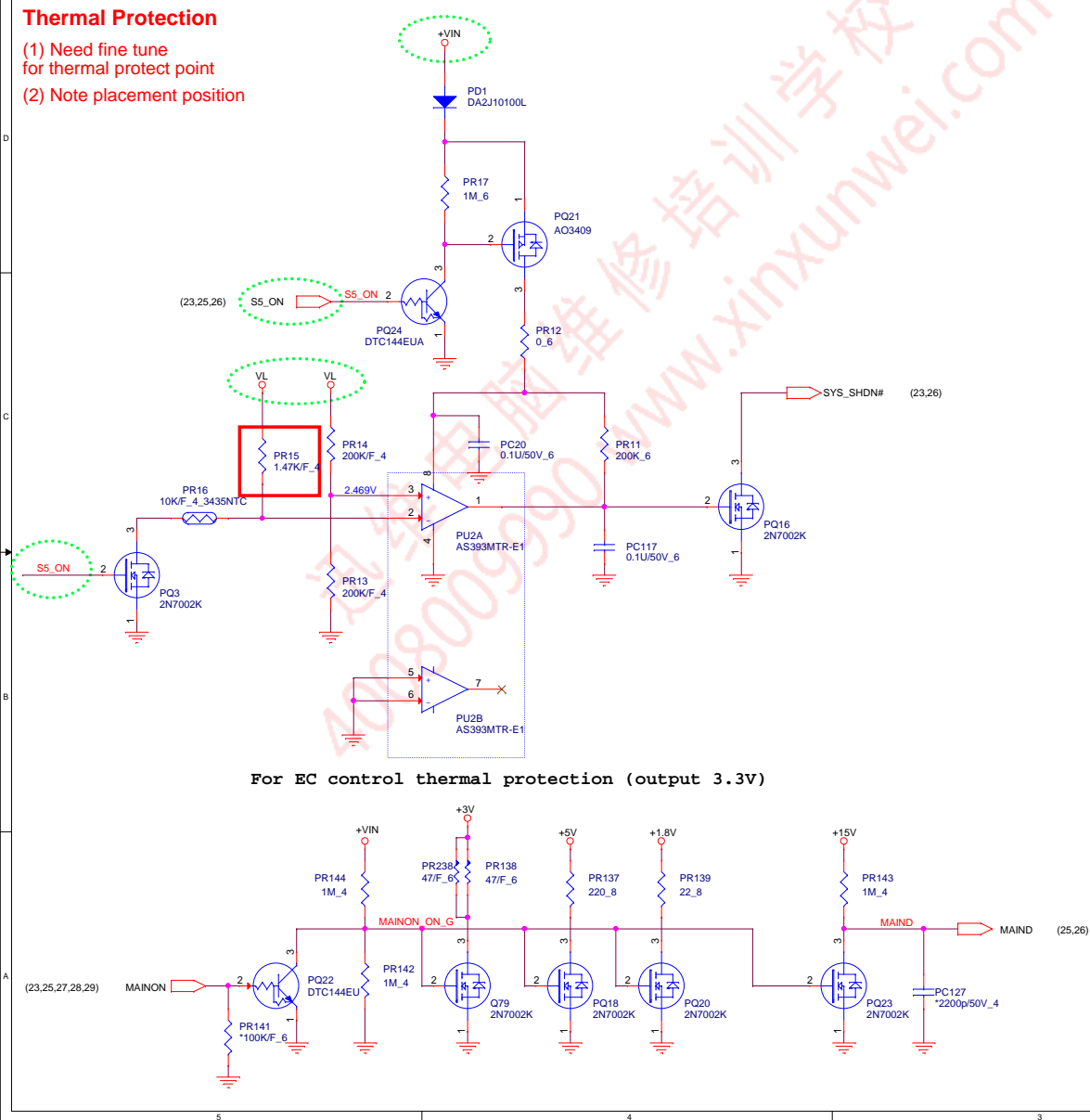
Parallel


Change RT8171BGQW to RT8175AGQW

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Thermal Protection

- (1) Need fine tune for thermal protect point
- (2) Note placement position




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Model	Rev.	CHANGE LIST			
ZHKD	1A	2014/12/11 First Release			

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DOC NO.	PROJECT MODEL :	ZHKD	APPROVED BY:	DATE:
	PART NUMBER:		DRAWING BY:	REVISION:


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 PROJECT : ZHW_2008
 Change list-1
 Date: 2014.12.11